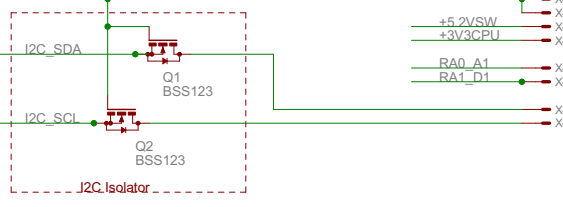
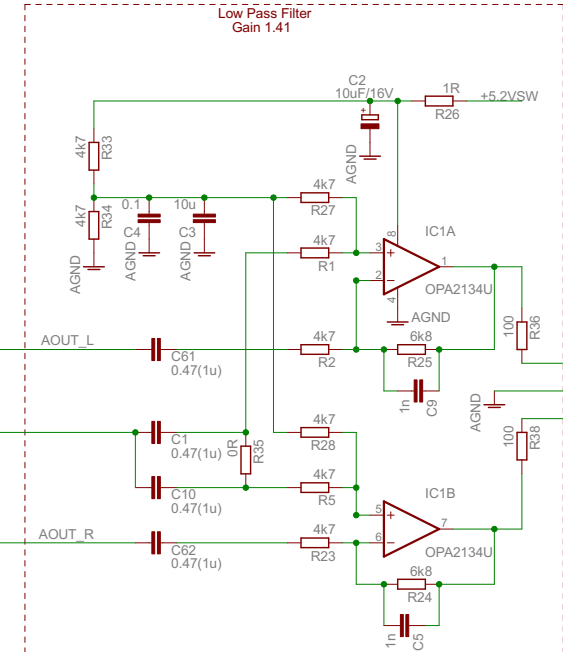
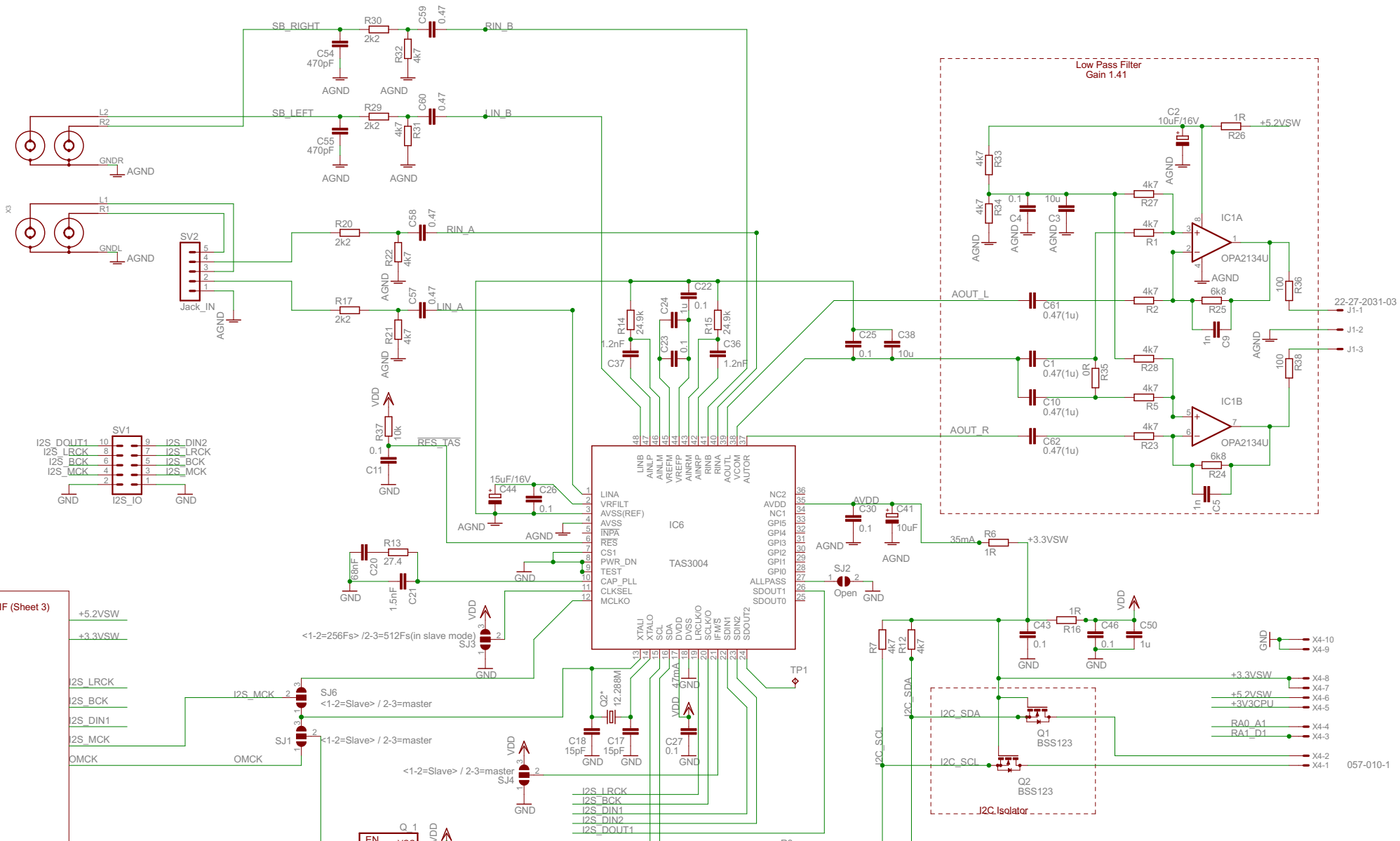


CS8416 Setup				
Address	Name	Bit name	Value	Obs.
0x00	Control_0	0_FSWCLK_0_0_PDUR_TRUNC_Reserved_Reserved	0b00001000	Clock signal on OMCK is output on RMCK according to the SWCLK bit <small>enable/force per external block/force or disable the DSP</small> Higher Update Rate Phase Detector
0x01	Control_1	SWCLK_MUTSAO_INT1_INT0_HOLD1_HOLD0_RMCKF_CHS	0b10001000	OMCK clock input is automatically output on RMCK on PLL Unlock RMCK output frequency is 256*Fs
0x02	Control_2	DETC1_EMPH_CN_TL2_0_GPO0SEL3_0	0b00000101	gpo0=RERR(receiver error)
0x03	Control_3	GPO1SEL3_0_GPO2SEL3_0	0b10011100	gpo1=Non Audio , gpo2 =H
0x04	Control_4	RUN_RXD_RXSEL2_0_TXSEL2_0	0b10011000	Normal Operation, RXD=0 ->RMCK is an output, Tx=RXPO RXPO input selected [011]
0x05	Ser. Audio Data Format	SOMS, SOSF, SORES1, SORES0, SOJUST, SODEL, SOSPOL, SOLRPOL	0b00000101	Audio Port is Slave, output frequency is 64*Fs, Audio output resolution is 24bit Left Justified, Delay 1CLK, SDOUT is sampled on rising edges of OSCLK SDOUT data is valid for the right channel when OLRCK is high
0x06	Receiver Error Mask	0_QCRCM_CCRCM_UNLOCKM_VM_CONFM_BIPM_PARM	0xFF	error not masked
0x07	Interrupt Mask	0_PCCHM_OSLIPM_DETCM_CCHM_RERRM_QCHM_FCHM	0x00	
0x08	Interrupt Mode MSB	0_PCCH1_OSLIP1_DETC1_CCH1_RERR1_QCH1_FCH1	0x00	
0x09	Interrupt Mode LSB	0_PCCH0_OSLIP0_DETC0_CCH0_RERR0_QCH0_FCH0	0x00	

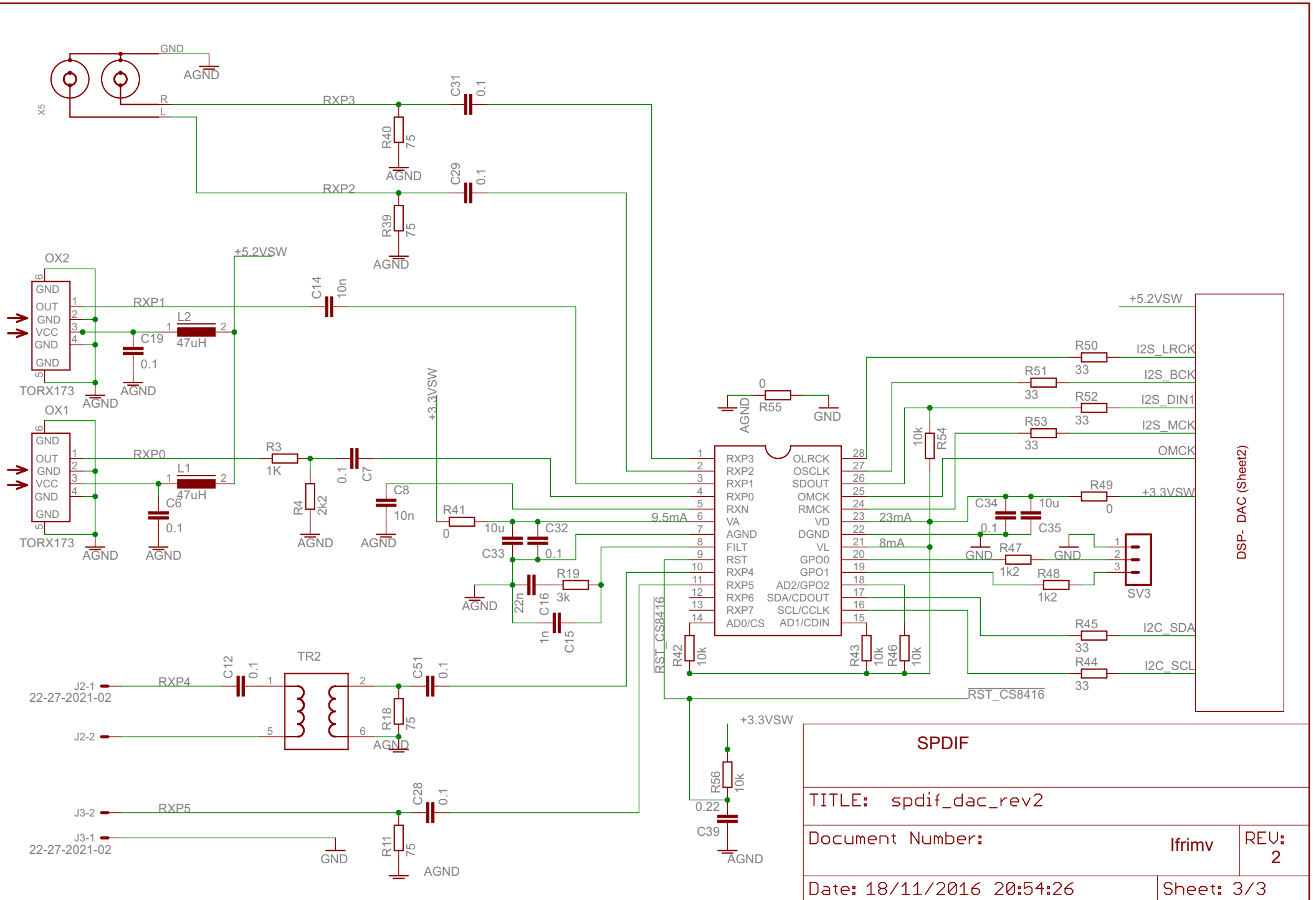
Block connection and setup info		
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ADC - DSP - DAC		
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J1-2
J1-3
X4-10
X4-9
X4-8
X4-7
X4-6
X4-5
X4-4
X4-3
X4-2
X4-1

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DSP- DAC (Sheet2)

SPDIF

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